IDEC Chip Design Contest

A Low In-Band Noise Sub-Harmonically Injection Locked PLL with Sub-Sampling

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Introduction

In general, the most modern SoCs such as micro-processors and wireless radio systems require several frequency synthesizers. The phase locked loops (PLL) is a promising solution for SoCs because of their low-power and wide frequency range characteristics. Therefore, the demand for low-jitter PLL with low-area and low-power consumption is increasing. However, noise performance is a trade-off between area and power consumption.

One of two main approaches to achieve noise specification is sub-sampling PLL (SSPLL). In a conventional PFD/CP PLL, the noise of PFD/CP is multiplied by N^2 because the divider is used to detect the frequency difference between the reference clock, Ref, and VCO output. In other words, in SSPLL, the phase error is estimated by sampling-sampling phase detector (SSPD). The SSPD converts the phase error into sampled voltage difference by sampling the VCO output with Ref and so has higher gain due to the high slew-rate of VCO output.

Another architecture is a sub-harmonically locked PLL (SILPLL) which mitigate not only in-band noise but also out-band noise. Owing to the out-band noise reduction effect, ring oscillator-based low noise PLLs can be implemented without excessive budgets outlays. Despite the advantage of ultra-low-noise, the SILPLL suffer from a critical issue from injection. The SILPLL delivers low-noise characteristic only when the frequency difference between the free-running frequency of VCO, f_{free}, and $N \cdot f_{ref}$ is quite small where N and f_{ref} are division ratio and the frequency of reference, respectively.

Sub-harmonically Injection Locked PLL

The phase offset issue between the FLL and injection, the SILPLL still retains the great advantage of low-noise. As shown in Figure 1, the ring VCO can be implemented with an injection switch. The signal which has the lowest noise in system periodically corrects the output of VCO. In Figure 1, the differential signal is shorted by injection pulse. Then, the phase of ring VCO is aligned by injection pulse as shown in Figure 2. (a). In the ring VCO, the output of the VCO is fed to the VCO as an input. Thus, the jitter accumulates as it goes through the stage. The noise performance is improved because the accumulated jitter is initialized by injection. In detailed, the phase pulling and pushing mechanism for jitter initialization is also described in Figure 2. (b). In general, the ring VCO occupies a small silicon area instead of inferior noise performance than LC VCO. Therefore, the low noise ring VCO can be implemented without an inductor which requires a large silicon area.

The phase of VCO and injection is simultaneously aligned after frequency and phase locking. However, the phase of the two signals is slightly different due to noise. At this time, the phase of VCO is shifted in proportion to the phase error. this ratio is defined as the injection factor, α, which is decided by the injection current. The phase domain model of the conventional SILPLL is modeled in Figure 3. The transfer function of injection, $H_{inj}(j\omega)$, and up-conversion of the reference clock, $H_{up}(j\omega)$, is expressed as follow

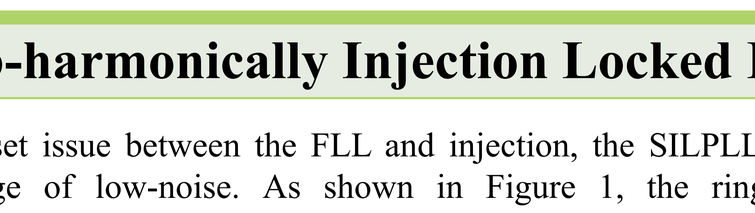

Figure 1. Ring VCO with injection switch

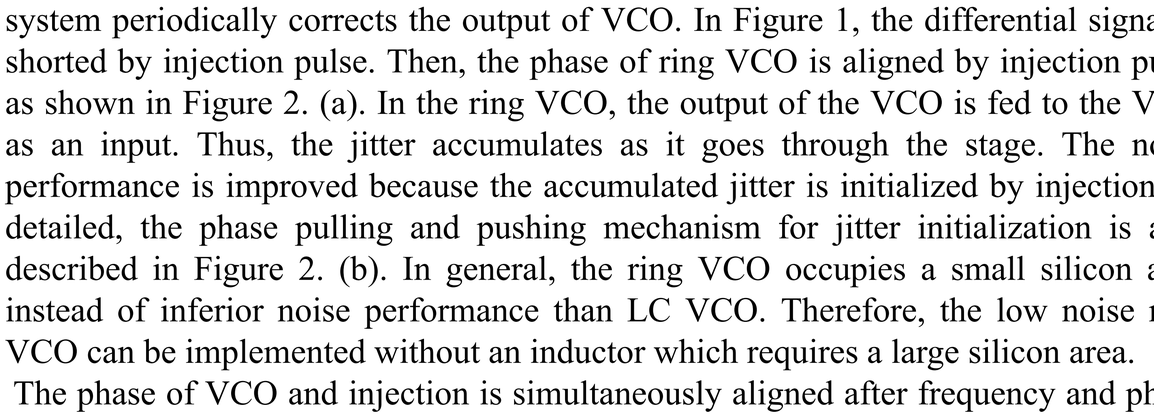

Figure 2. (a) Accumulated jitter reset and (b) phase pulling/pushing

$$H_{inj}(j\omega) = 1 - \frac{\alpha}{1+(\alpha-1)e^{-j\omega T_R}} e^{-j\omega T_R/2} \frac{\sin(\omega T_R/2)}{\omega T_R/2} \quad (1)$$

$$H_{up}(j\omega) = 1 - \frac{N\alpha}{1+(\alpha-1)e^{-j\omega T_R}} e^{-j\omega T_R/2} \frac{\sin(\omega T_R/2)}{\omega T_R/2} \quad (2)$$

In Figure 4, the transfer function of VCO and PFD/CP is shown and α=0,1 represent PFD/CP PLL without injection and ideal injection, respectively. The value of N and I_{CP} for $K_{d,PFD/CP}$ are 32 and 50 uA, the same as this work. The out-band noise of the VCO is effectively reduced by injection until the locking frequency in Figure 4. (a). However, as shown in Figure 4. (b), the in-band noise of PFD/CP suffers from insufficient noise reduction even though high α is used. Specifically, the ideal injection provides only 3.5 dB reduction at 1 kHz.

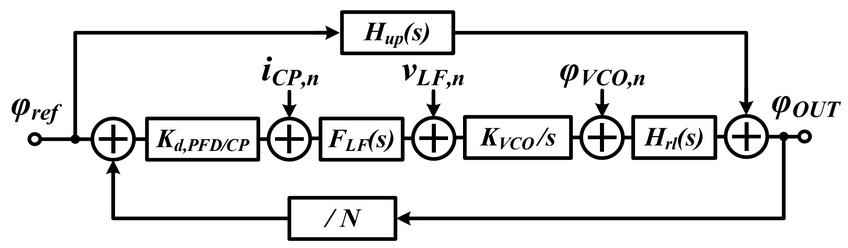

Figure 3. Linear phase domain model of SILPLL

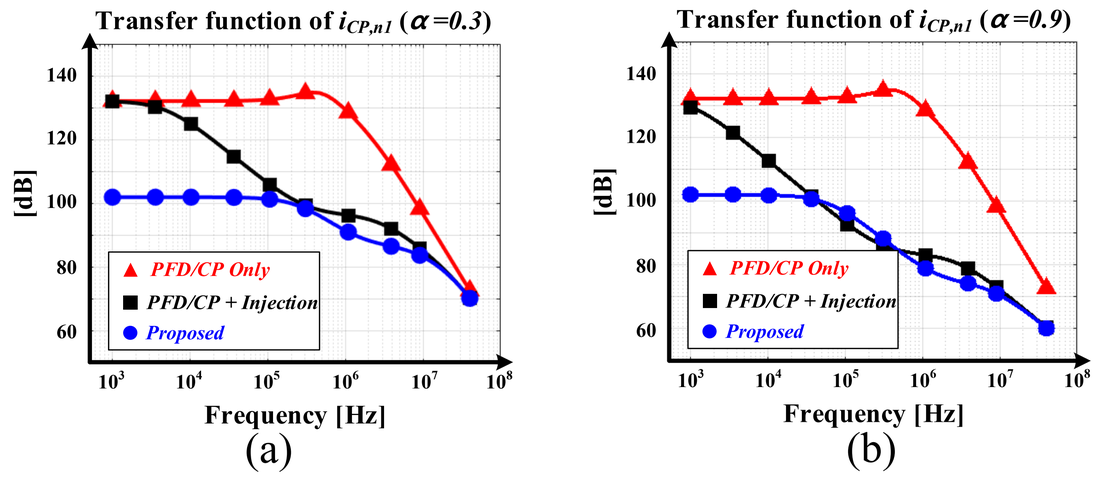

Figure 4. Transfer function of (a) VCO noise and (b) PFD/CP noise with difference α

Measurement Results

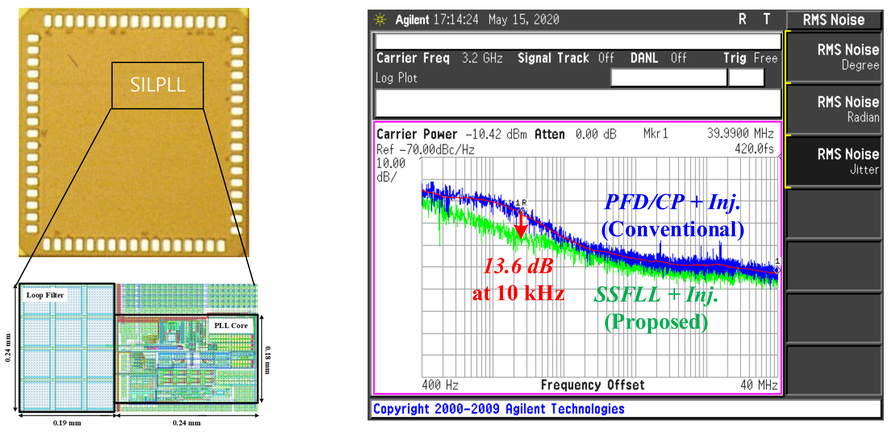

Figure 5. Die photo and measured phase noise of PFD/CP +*inj.* and SSFLL +*inj*. PLL

The proposed SILPLL is fabricated within a 65 nm CMOS process. A 100 MHz reference clock is used and a 3.2 GHz output is generated by the proposed SILPLL. The Figure 5 shows the measured phase noise spectrum of both the conventional SILPLL and the proposed SILPLL. The proposed SILPLL sufficiently reduces in-band noise. At 10 kHz offset, the phase noise of conventional and proposed SILPLL are -96.5 dBc/Hz and -110.1 dBc/Hz, respectively. As a result, the measure integrated jitter from 10 kHz to 40 MHz of the proposed SILPLL is 239 fs which is an improvement of 43% from 420 fs.

Acknowledgement

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